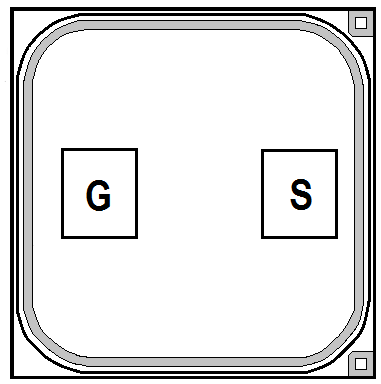
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.030”**

**.030”**

**CHIP BACK IS DRAIN**

**Top Material: Al**

**Backside Material: Ag**

**Bond Pad Size: .005” X .005”**

**Backside Potential: Drain**

**Mask Ref: G19**

**APPROVED BY: DK DIE SIZE .030” X .030” DATE: 10/5/22**

**MFG: ZETEX THICKNESS .010” P/N: ZVP3310**

**DG 10.1.2**

#### Rev B, 7/19/02